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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,204	04/21/2004	Richard S. Wise	FIS920030028	3203
32074	7590	10/16/2006	EXAMINER	
INTERNATIONAL BUSINESS MACHINES CORPORATION DEPT. 18G BLDG. 300-482 2070 ROUTE 52 HOPEWELL JUNCTION, NY 12533			MALDONADO, JULIO J	
			ART UNIT	PAPER NUMBER
			2823	

DATE MAILED: 10/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 8 and 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (U.S. 6,228,763 B1) in view of Zhao (U.S. 6,211,561 B1) and Chiang et al. (U.S. 5,817,572, hereinafter Chiang).

Lee (Figs.3A-3D) teaches an wiring structure including a first dielectric layer (300, 302), wherein said first dielectric layer (300, 302) further includes an interlayer dielectric (300) and an etch stop layer made of silicon nitride; a plurality of conductors (312) disposed on said first dielectric layer (300, 302), said conductors (312) separated laterally from each other by portions of the first dielectric layer (300, 302) and portions of a second dielectric layer (306) and by air gaps (314), each of the conductors (312) having air gaps (314) adjacent thereto separating the conductor (312) from the first dielectric layer (300, 302) and the second dielectric layer (306); and a third dielectric layer (316) overlying the conductors (312), wherein each of said conductors (312) has a cross-section wider at a top thereof than at a bottom thereof, in accordance with each of the air gaps (314) having a cross-section wider at a bottom thereof than at a top thereof and wherein the first dielectric layer (300, 302) further includes a contacting stud (304)

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in contact with said conductor (312) (column 1, lines 41 – 52, column 2, lines 18 – 21, and column 4, line 25 – column 5, line 28).

Lee fails to disclose wherein said first dielectric layer and said third dielectric layer each have a dielectric constant less than that of the second dielectric layer. However, Zhao (Fig.1A) teaches an interconnect structure including a first dielectric layer (12) having interconnects therein; a metal line (16, 30) formed on said first dielectric layer (12); a second dielectric layer (18) made of SiO₂ or low-k dielectric materials; and a third dielectric layer (26) made of SiO₂ or low-k dielectric materials such as polyimides, parylene and fluoropolymers, wherein said second dielectric layer (18) have air gaps (22) therein (Zhao, column 3, line 54 – column 8, line 60).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Lee and Zhao to enable the second and third dielectric layers of Lee to be made of the materials of Zhao because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable materials for the dielectric layers of Lee and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Although the combination of Lee and Zhao teach a third dielectric layer having a dielectric constant lower than that of the second dielectric layer and wherein the first dielectric layer further includes interconnects, the combined teachings of Lee and Zhao fail to disclose wherein the first dielectric layer has a dielectric constant lower than that of the second dielectric layer. However, Chiang (Figs.4 and 25) teaches an interconnect structure formed on substrate (20) including multiple interlayer dielectric

layers (22, 23 in Fig.4, and 322, 323 in Fig.25), wherein said multiple interlayer dielectric layer (22, 23) further includes an interlayer dielectric (22) made of SiO₂, fluoropolymer, polyimides, and an etch stop layer (23) made of either silicon nitride or boron nitride (Chiang, column 6, lines 48 – 65). It would have been within the scope of one of ordinary skill in the art to combine the teachings of Lee and Zhao with Chiang to enable the dielectric layer of the interconnect structure of Lee and Zhao to be made using the materials disclosed in Chiang because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable materials for the first dielectric layer of Lee and Zhao and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

Response to Arguments

Applicants argue, "...Amended independent claim 8 recites a wiring structure having conductors, inter alia, "disposed on said first dielectric layer, said conductors separated laterally from each other by portions of the first dielectric layer and portions of a second dielectric layer and by air gaps, each of the conductors having air gaps adjacent thereto separating the conductor from the first dielectric layer and the second dielectric layer". Applicants respectfully submit that prior art references of record, in particular, Lee, Zhao, and/or Chiang et al., alone or in combination, do not teach, suggest, or even imply the above quoted distinctive elements of independent claim 8...". In response to this argument, as explained in the rejection included in this office action, Lee teaches an wiring structure including a first dielectric layer (300, 302), wherein said first dielectric layer (300, 302) further includes an interlayer dielectric (300) and an etch

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stop layer made of silicon nitride (column 1, lines 41 – 52, column 2, lines 18 – 21, and column 4, line 25 – column 5, line 28).

Conclusion

3. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

4. Applicants are encouraged, where appropriate, to check Patent Application Information Retrieval (PAIR) (<http://portal.uspto.gov/external/portal/pair>) which provides applicants direct secure access to their own patent application status information, as well as to general patent information publicly available.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Julio J. Maldonado whose telephone number is (571) 272-1864. The examiner can normally be reached on Monday through Friday.

6. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (571) 272-1907. The fax number for this

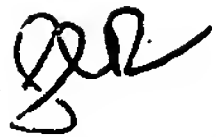
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group is 571-273-8300. Updates can be found at

<http://www.uspto.gov/web/info/2800.htm>.



Julio J. Maldonado
October 4, 2006

Julio J. Maldonado
Patent Examiner
Art Unit 2823



GEORGE R. FOURSON
PRIMARY EXAMINER